

REMARKS

I. Introduction

As a preliminary matter, it is noted that the Examiner has not provided an initialed copy of the Information Disclosure Statement filed on August 27, 2003. A copy of the IDS and stamped-post card showing receipt by the PTO is attached hereto for the Examiner's convenience. It is respectfully requested that the Examiner provide Applicants an initialed copy of the IDS indicating that each of the prior art references cited therein have been considered and made of record.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-3 Under 35 U.S.C. § 103

Claims 1-3 are rejected under 35 U.S.C. § 103 as being unpatentable over Applicants' Admitted Prior Art ("AAPA") in view of USP No. 6,512,263 to Yuan. Applicants respectfully traverse this rejection for at least the following reasons.

Conventionally, as described in the AAPA section of Applicants' specification, when the second polysilicon film 210A and the parts of the sidewall-shaped polysilicon films 210B located over the shallow trench isolations (STIs) 202 are removed using the mask pattern 212, an anisotropic etching process is carried out so as to obtain the floating gate electrodes 210C via the sidewall-shaped polysilicon films 210B. Specifically, the upper face of the second polysilicon film 210A on the STIs 202 has a height much higher than the thickness of the control gate electrodes 204, the first insulating films 205 and the second polysilicon film 210A. However, Applicants have discovered that when the second polysilicon film 210A is etched, the etch

selectivity of the second polysilicon film 210A to the second silicon dioxide film 209 is high. As a result, the second silicon dioxide film 209 exposed in the regions 201b having a small thickness partially breaks. Consequently, the semiconductor substrate 201 is also etched during the etching process, rendering a disconnection in the doped layer between the STIs 202.

In view of the foregoing problem and in accordance with one exemplary embodiment of the present invention, the isolations are spaced apart from each other along the width of the control gate electrodes. In particular, each of the isolations extends continuously along the length of the control gate electrodes, so that the control gate electrodes, which function as a memory controlling implantation to draw off charges from the floating gate electrodes and serve as a *word line* in the memory cell array, can be connected to the memory cells (see, e.g., 2 of Fig. 1 and 12 of Fig. 9 of Applicants' drawings). Accordingly, because a portion of the second polysilicon film for forming the floating gate electrodes is removed from the isolations in a process step while the remaining portion of the second polysilicon film are removed from the source regions in another process step, the etching of the semiconductor substrate and the disconnections between the doped regions are advantageously prevented when an etching process is carried out to form the floating gate electrodes (see, e.g., page 8, lines 11-21 of the specification).

In the pending Office Action, the Examiner admits that the AAPA does not disclose or suggest that the isolations 202 extend continuously along the length of the control gate electrodes 204. The rejection asserts that the conductive lines 49/51/53 of Yuan "are crossed by the isolation trenches 72/73/74 that extend continuously along their length."

However, it is respectfully submitted that the Examiner's conclusion is incorrect. Specifically, the conductive lines 49/51/53 of Yuan across the isolations 72/73/74 extending in

the column direction merely function as electrical conductive ***bit lines*** (see, col. 6, lines 53-67). As such, the conductive lines 49/51/53 of Yuan do not correspond to the claimed control gate electrodes, let alone contain a structural layout as recited by the pending claims.

Furthermore, as illustrated in Fig. 8 of Yuan, the transistor T2 to which the word line 91 is connected has a substantially different configuration than the transistors T1-Left and T1-Right having a memory function to which the conductive bit lines 49' and 51' are connected. It is important to note that the transistors T1-Left and T1-Right having the memory function are respectively controlled by the Left-Steering Gate 82' and the Right-Steering Gate 83', rather than by the Select/Erase Word Line Gate 97' (see, col. 7, lines 17-47). Therefore, as the conductive lines 49/51/53 of Yuan are merely bit lines and not word lines, it is respectfully submitted that the Examiner's proposed combination is improper.

Even assuming *arguendo* that the Examiner's interpretation is proper, the cited prior art is completely silent as to the problems related to the disconnection in the doped layer located between the STIs or the semiconductor substrate 201 being etched unintentionally, let alone the means by which to solve such problems as conceived by Applicants. Indeed, it is respectfully submitted that the alleged motivation for making the combination is not derived from the prior art, but rather perhaps subconsciously, is based solely on improper hindsight reasoning utilizing the Applicant's specification.

For example, the Examiner alleges that "it would have been obvious to someone with ordinary skill ...to modify [the AAPA]...in order to provide a high-degree of electrical isolation between the rows and cells, as well as increase the data density of the memory device (see, page 3 of Office Action." However, there is no evidence from the cited prior art for supporting the alleged motivation. Indeed, the AAPA does not appear to discuss or even recognize any lack of

electrical isolation between any rows or cells, let alone provide a means to overcome such problem. Only Applicants have conceived and enabled, and developed the motivation for preventing the substrate from being unintentionally etched while maintaining the connection between the STIs in the doped regions.

Finally, in the event it is asserted that the word lines 91-94 of Yuan correspond to the claimed control gate electrodes, it is noted that the isolations 72/73/74 are *in parallel* with the word line 91, and as such, they clearly do not *cross* any of the word lines 91-94. Accordingly, such an interpretation of Yuan still fails to arrive at the claimed invention.

In the foregoing hypothetical scenario, if the word line 91 extending in parallel with the alleged isolations 72/73/74 (see, Exhibit A) is modified to extend in a direction crossing the alleged isolations (see, Exhibit B), the selected cell can no longer be independently read or controlled by the Left-Steering Gate, Right-Steering Gate or the Select/Erase Word Line Gate, because the transistors arranged in the parallel direction are now modified to connect to the same word line. Accordingly, not only is there no disclosed need or desire for modifying the word line 91 to extend in a direction crossing the alleged isolations, doing so would effectively prevent the memory cells from operating as intended by Yuan. It is important to note that the word lines of Yuan are not designed to extend in the column direction, but rather, designed to extend along the row of the array 11 of the cells so as to electrically connect through lines 17 to a word line decoder and driver circuit 19 (see, col. 4, lines 60-63), such that the trenches 72/73/74 may be positioned therebetween (see, col. 6, lines 14-16 and lines 34-42).

In view of the foregoing, it is clear that the cited prior art is silent as to the features recited in claim 1, let alone the other features recited in the dependent claims. Accordingly, it is submitted that claim 1 is patentable over the AAPA in combination with Yuan.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Application No.: 10/648,515

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

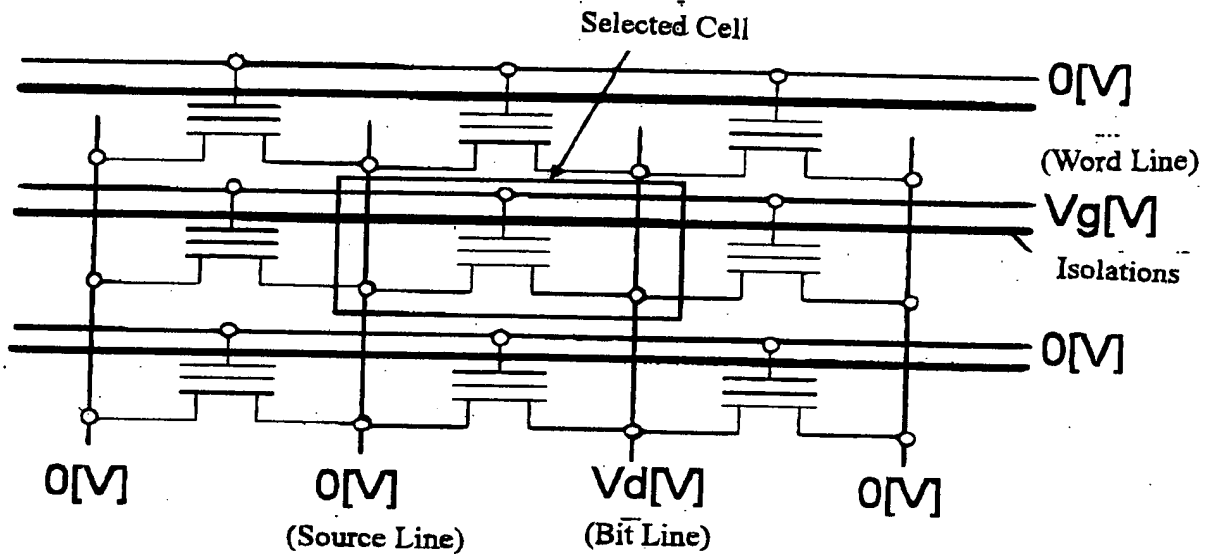
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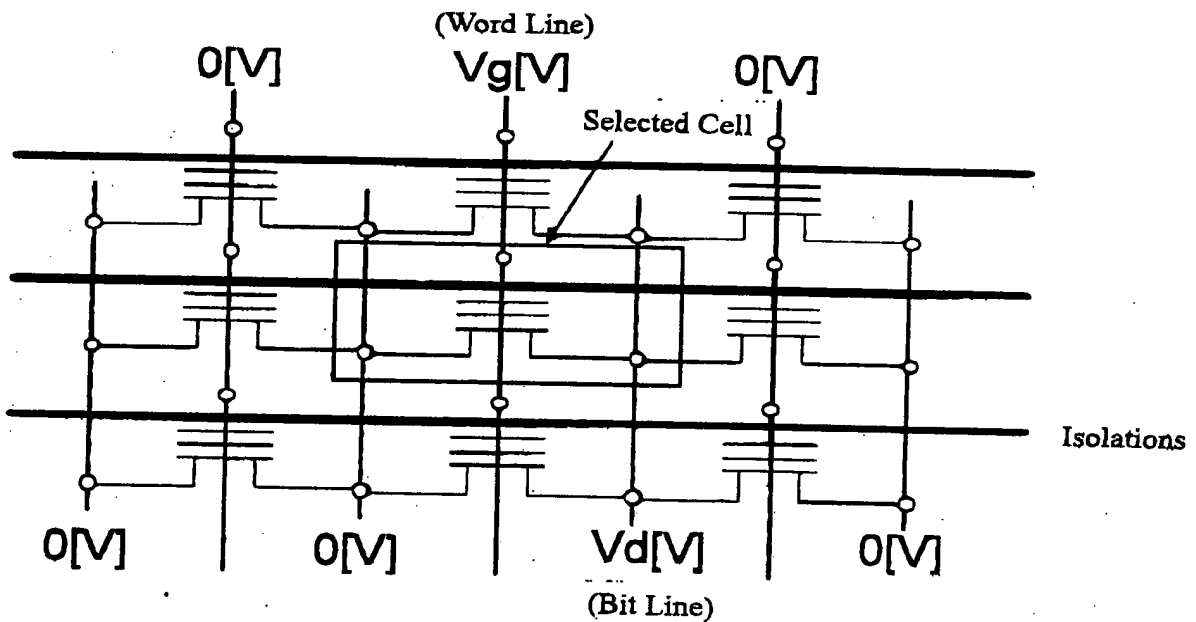
Yuan (Word line in parallel to isolations)

Only the selected cell can be read because the transistors arranged in a vertical direction are connected to different word lines to be controlled independently.



Yuan & AAPA (Word line crossing isolations)

Exhibit A



The selected cell can not independently be read because the transistors arranged in a vertical direction are connected to the same word line, so as not to be controlled independently.

Exhibit B